IN THE CLAIMS:

Claim 1 (previously presented): A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,

each of the alignment marks being divided by a micronized pattern,

the micronized pattern having a size smaller than a resolution limit of an alignment sensor, and

the micronized pattern having a pattern forming margin larger than that of a device pattern formed over the semiconductor wafer has.

Claim 2 (original): A semiconductor device according to claim 1, wherein

the micronized pattern is a line-and-space pattern.

Claim 3 (previously presented): A semiconductor device according to claim 2, wherein

each of lines constituting the line-and-space pattern are divided into a plurality of segments.

Claim 4 (previously presented): A semiconductor device according to claim 3, wherein

positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines.

Claims 5-12 (canceled):

Claim 13 (currently amended): A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,

each of the alignment marks being divided by a micronized line-and-space pattern into a

plurality of lines extending along a first direction, and

each of the plural lines ~~constituting the line-and-space pattern~~ being divided in a second direction perpendicular to the first direction into a plurality of segments.

Claim 14 (previously presented): A semiconductor device according to claim 13, wherein positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines.

Claim 15 (previously presented): A semiconductor device according to claim 13, wherein a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.

Claim 16 (previously presented): A semiconductor device according to claim 14, wherein a margin for forming the micronized pattern to be formed in is larger than a margin for a device pattern to be formed on the semiconductor wafer.